Weighted Median Filter Architecture Based on the Sparse Window Approach

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Abstract. The weighted median filter (WMF) is widely used for disparity refinement in stereo vision. Various studies have been conducted to implement the WMF as hardware. In particular, the separable weighted median filter (sWMF), which reduces complexity by separating the 2-dimensional WMF into two 1-dimensional WMFs, has been proposed for implementation as hardware. By improving the sWMF, this paper proposes an architecture that uses fewer hardware resources than the sWMF.

1 Introduction

Because the weighted median filter (WMF) can eliminate noise efficiently while preserving edge areas, it is widely used for disparity refinement in stereo vision [1, 2]. Various studies have been conducted to improve real-time performance of the WMF by hardware implementation. In general, implementing the WMF as hardware is difficult because its complexity tends to increase by $O(r^2)$ as the window radius r increases [1, 2]. To efficiently implement the WMF as hardware, the separable weighted median filter (sWMF) has been proposed [1]. The main idea of the sWMF is to divide the 2-dimensional WMF into cascaded 1-dimenional (1-D) horizontal and vertical WMFs to reduce the computational complexity to $O(r)$. In this paper, by using the sparse window approach [3], we propose an architecture that uses fewer hardware resources than the sWMF while maintaining the complexity $O(r)$.

2 Proposed Architecture

Increasing the window size of the WMF, as applied to disparity refinement of stereo vision, tends to decrease the disparity error rate. As the window size increases, however, the hardware complexity of the WMF increases as well. Thus, this paper proposes an architecture in which the horizontal WMF adopts the sparse window approach. The proposed architecture reduces hardware resources or decreases the disparity error rate by using the sparse window with horizontal size m that provides a similar effect to the original window with horizontal size $2m–1$.

As shown in Fig. 1(a), the proposed architecture consists of a 1-D horizontal weighted median filter (HWMF), line buffers, and a 1-D vertical weighted median filter (VWMF). Unlike the sWMF, the proposed 1-D HWMF uses a sparse window to find the weighted median value. Fig. 1(b) shows the module to generate the horizontal sparse window. The disparity and image inputs to the 1-D HWMF are split into even or odd windows depending on their *x* coordinates, and then each window is sent to the corresponding sorter. To sort the disparity values, the 1-D HWMF and 1-D VWMF use linear sorters, each of which consists of a sorting basic cell (SBC) array [4]. Similar to the sWMF, the weight calculator computes the weights based on the difference of values between the center pixel and the others in the window of the original image. The weight calculator also accumulates each weight in order by using an adder tree. It then sends the accumulated weights and the total weight sum, T_W, to the median selector. The median selector compares each accumulated weight to the $T_w/2$, and generates a string of 0's and 1's by giving a "0" if the accumulated weight is smaller, and a "1" if it is equal or larger. The position of the first "1" in the string indicates the position of a disparity selected as the median value. The main difference between the 1-D HWMF and 1-D VWMF in the proposed architecture is that the sparse window approach is applied in the former and not in the latter. In addition, the 1-D VWMF should be implemented by including several line buffers. Except for these, the operations of the 1-D VWMF are almost identical to those of the 1-D HWMF. For simultaneous read and write operations, the line buffers are constructed with dual-port RAMs.

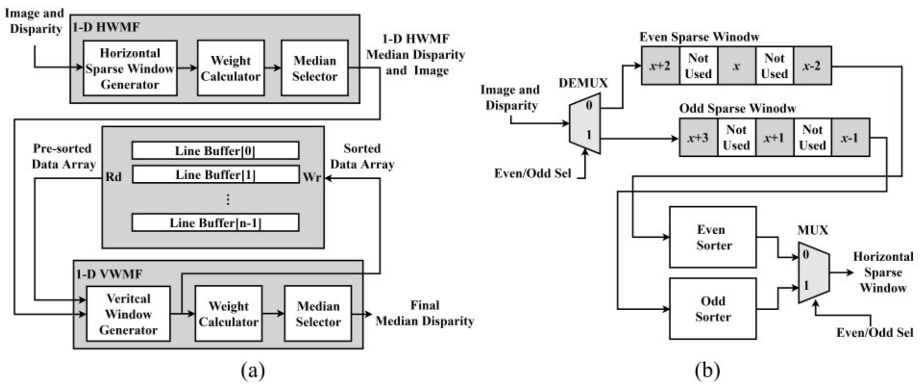

Fig. 1. Proposed architecture: (a) overall architecture; and (b) horizontal sparse window generator.

Table 1. Comparison of synthesis results between the proposed architecture and sWMF.

Architecture	Window Size	Slice LUTs	Slice Registers	DSP48Es	Block RAM
sWMF	39 × 39	12,200/203,800	15,813/407,600	0/840	55/445
Proposed	21 × 39	13,668/203,800	8,319/407,600	0/840	58.5/445
	39 × 39	22,268/203,800	11,688/407,600	0/840	58.5/445

3 Experimental Results

The proposed architecture was implemented on a Xilinx XC7K325T FPGA to be compared with the sWMF. Both architectures used 148.5 MHz as the working frequency and 128 as the disparity range. The maximum video format for both architectures is 1080p@60Hz. Table 1 shows the comparison of synthesis results between the proposed architecture and the sWMF. In the proposed architecture whose window size is 21 × 39, the horizontal sparse window is made by selecting sparsely 21 pixels among 41 horizontal pixels. In this case, when compared with the sWMF, the proposed architecture reduces the number of Slice Registers by nearly half while slightly increasing the hardware resource usage of Slice LUTs and Block RAMs. In the proposed architecture whose window size was 39 × 39, the hardware resource usage of Slice LUTs increases but the disparity error rate can be decreased.

4 Conclusion

In this paper, we proposed a hardware-friendly architecture for the WMF using the sparse window approach. The proposed architecture can reduce the hardware resource usage as compared with the sWMF by generating horizontal sparse windows. Because of this advantage, the proposed WMF architecture can be widely used for disparity refinement in stereo vision. In future work, we will evaluate the disparity refinement performance of the proposed architecture.

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